Notice of Allowability	Application No.	Applicant(s)	
	09/241,695	MIYANAGA ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the 6-22-04 amendment*.

2. ☒ The allowed claim(s) is/are *1,15,18,21,24,28-33,42-47 and 56-58*.

3. ☒ The drawings filed on *24 June 2004* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20040916* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Mark Murphy (RN: 34,225) on September 16, 2004.

The application has been amended as follows:

IN THE CLAIMS

1. (Currently amended) A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and in the source region,

wherein the impurity region extends in a direction of the <100> axis ~~on~~ in the {100} plane of the single crystal semiconductor substrate,

wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate,

wherein the impurity region is not in contact with the drain region, and

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region formed under the channel forming region and in the source region, and

wherein the impurity region is formed through implantation along a direction of the <110> axis with respect to the semiconductor substrate with a gate electrode as a mask.

2-14 (Canceled)

15. (Original) A device according to claim 1, wherein the semiconductor device is an integrated circuit (IC).

16-17. (Canceled)

18. (Original) A device according to claim 1, wherein the semiconductor device is a microprocessor.

19-20. (Canceled)

21. (Original) A device according to claim 18, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

22-23. (Canceled)

24. (Original) A device according to claim 1, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

25 - 27. (Canceled)

28. (Previously presented) A device according to claim 1, wherein the single crystal semiconductor substrate is a single silicon substrate.

29. (Currently amended) A semiconductor device comprising a plurality of MOSFETs formed in a single crystal semiconductor substrate,

each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region;

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and in the source region;

a pair of LDD regions, wherein one of the pair of LDD regions is formed between the source region and the channel forming region while the other of the pair of LDD regions is formed between the channel forming region and the drain region,

wherein the impurity region extends in a direction of the <100> axis ~~on~~ in the {100} plane of the single crystal semiconductor substrate,

wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate,

wherein the impurity region is not in contact with the drain region, and

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region formed under the channel forming region and in the source region, and

wherein the impurity region is formed through implantation along a direction of the <110> axis with respect to the semiconductor substrate with a gate electrode as a mask.

30. (Previously presented) A device according to claim 29, wherein the semiconductor device is an integrated circuit (IC).

31. (Previously presented) A device according to claim 29, wherein the semiconductor device is a microprocessor.

32. (Previously presented) A device according to claim 31, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

33. (Previously presented) A device according to claim 29, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

34. (Canceled)

35-41. (Canceled)

42. (Currently amended) A semiconductor device comprising at least a CMOS circuit including an n-channel MOSFET and a p-channel MOSFET each being formed in a single crystal semiconductor substrate,

said n-channel MOSFET comprising:

a first source region and a first drain region each comprising a first n-type impurity;

a first channel forming region being formed between the first source region and the first drain region;

a first impurity region including a first p-type impurity and being formed under the first channel forming region and in the first source region;

wherein the first impurity region is not in contact with the first drain region,

said p-channel MOSFET comprising:

a second source region and a second drain region each comprising a second p-type impurity;

a second channel forming region being formed between the second source region and the second drain region;

a second impurity region including a second n-type impurity and being formed under the second channel forming region,

wherein each of the first impurity region and the second impurity region extends in a direction of the <100> axis ~~on~~ in the {100} plane of the single crystal semiconductor substrate,

wherein each of the first and second impurity regions is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate, and

wherein each of the first and second impurity regions is formed through implantation along a direction of the <110> axis with respect to the semiconductor substrate with a corresponding gate electrode as a mask.

43. (Previously presented) A device according to claim 42,

wherein the first n-type impurity is arsenic,

wherein the second n-type impurity is phosphorus,

wherein each of the first and second p-type impurity is boron.

44. (Previously presented) A device according to claim 42, wherein the semiconductor device is an integrated circuit (IC).

45. (Previously presented) A device according to claim 42, wherein the semiconductor device is a microprocessor.

46. (Previously presented) A device according to claim 45, wherein the microprocessor is at least one selected from the group consisting of a RISC processor and an ASIC processor.

47. (Previously presented) A device according to claim 42, wherein the semiconductor device is at least one selected from the group consisting of a cellular phone, a personal handy phone system, and a portable computer.

48-49. (Canceled)

50-55. (Canceled)

56. (Currently amended) An EL display device comprising:

a plurality of MOSFETs formed in a single crystal semiconductor substrate, each of the plurality of MOSFETs comprising:

a source region and a drain region each including a first impurity;

a channel forming region being formed between the source region and the drain region; and

an impurity region including a second impurity having an opposite conductive type to the first impurity and being formed under the channel forming region and in the source region,

wherein the impurity region extends in a direction of the <100> axis ~~on~~ in the {100} plane of the single crystal semiconductor substrate,

wherein the impurity region is not in contact with the drain region,

wherein the impurity region is formed at a depth in a range of 20 to 150 nm from a surface of the single crystal semiconductor substrate,

wherein a concentration of the second impurity in the channel forming region is from 1/100 to 1/10 of that in the impurity region,

wherein the second impurity is introduced from a direction of the < 110 > axis with respect to the single crystal semiconductor substrate with a gate electrode as a mask, so that the second impurity is introduced from a perpendicular direction to a plane having the smallest atomic density of the single crystal semiconductor substrate,

wherein the concentration of the second impurity in the impurity region is in a range of 1×10^{18} to 1×10^{19} atoms/cm^3,

wherein the concentration of the second impurity in the channel forming region is in a range of 1×10^{16} to 1×10^{17} atoms/cm^3.

57. (Currently amended) An EL display device according to claim 56,

wherein the first impurity is arsenic or phosphorus, and

wherein the second impurity is ~~phosphorus~~ boron.

58. (Previously presented) An EL display device according to claim 56, wherein the EL display device is incorporated into at least one selected from the group consisting of a cellular phone, a personal handy phone system and a portable computer.

59. (Canceled)

Allowable Subject Matter

Claims 1, 15, 18, 21, 24, 28-33, 42-47 and 56-58 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
September 16, 2004

SHOUXIANG HU
PRIMARY EXAMINER